REMARKS

Claims 1-20 are pending in this application, of which claims 3-6, 8, 10, 12, 14, and 16-20 are withdrawn from consideration.

Enclosed Copy of *Wolf et al.* Is Incomplete

The Examiner cited the following reference in the Office Action mailed August 28, 2006: Stanley Wolf et al., "Silicon Processing for the VLSI Era," 2000, Volume 1, Lattice Press, 719-727, 791-795 ("*Wolf et al.*"). However, the copy of *Wolf et al.* that the Examiner enclosed with the Office Action is incomplete because it is missing page 795. For at least the reason that the Examiner cites page 795 of *Wolf et al.* in the Office Action, Applicants respectfully request that the Examiner send Applicants a complete copy of *Wolf et al.*

§ 103(a) Rejection of Claims 1, 2, 7, 9, 11, 13, and 15 over *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.*

Applicants respectfully traverse the rejection of claims 1, 2, 7, 9, 11, 13, and 15 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,994,762 to Suwanai et al. ("*Suwanai et al.*") in view of *Wolf et al.*, and further in view of U.S. Patent No. 6,770,977 to Kishida et al. ("*Kishida et al.*"). A *prima facie* case of obviousness has not been established.

To establish a *prima facie* case of obviousness under § 103(a), each of three requirements must be met. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art," to combine references or modify a reference. MPEP § 2143 (8th ed.

Rev. Feb. 2003). Second, a reasonable expectation of success must exist that the proposed modification will work for the intended purpose. *Id.* Moreover, both of these requirements must "be found in the prior art, not in applicant's disclosure." *Id.* Third, the reference or references, taken alone or in combination, must disclose or suggest every element recited in the claims. *Id.*

Claims 1, 2, 7, 9, 11, 13, and 15 are allowable over *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.* because these references fail to teach or suggest, either alone or in combination, each and every element of claim 1, from which claims 2, 7, 9, 11, 13, and 15 depend. For example, *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.* fail to teach, alone or in combination, a semiconductor device comprising, inter alia, "a conductor which covers a side face of the first insulating film at least near four corners of the semiconductor substrate ...; and a second insulating film covering [an] outer side face of the conductor," as recited in claim 1.

Suwanai et al. teaches a semiconductor integrated circuit device. As shown in Figure 11, the device has a "BPSG [(boron-doped phospho silicate glass)] film 17 and a silicon oxide film 27" (col. 7, line 66 to col. 8, line 2) that has been "deposited ... on the BPSG film 17" (col. 10, lines 21-22). "Further, a wiring 18 constituting a portion of the guard ring GR is formed on the silicon oxide film 27 at the outer circumference of the chip" (col. 8, lines 2-4). "[T]he wiring 18 is electrically connected with [a] semiconductor region 7 of [a] p-type well 2 through a connection hole 29 apertured in the silicon oxide film 27 and the BPSG film 17" (col. 8, lines 21-24). The device also has a "BPSG film 20" (col. 8, lines 25-27).

However, the wiring (18) in *Suwanai et al.* does not "cover[] a side face of" the BPSG film (17) or silicon oxide film (27), as required by claim 1. Rather, the wiring (18) is "formed on the silicon oxide film 27" (col. 8, lines 2-4; emphasis added). As explained above, the silicon oxide film (27) is "deposited ... on the BPSG film 17" (col. 10, lines 21-22; emphasis added). A wiring that is formed on a film does not constitute "a conductor which covers a side face of" the film, as required by claim 1 (emphasis added).

The connection of the wiring (18) to the semiconductor region (7) through the connection hole (29) also does not constitute the "conductor" recited in claim 1 because the connection hole (29) does not "cover[] a side face of" the BPSG film (17) or silicon oxide film (27) "at least near four corners," as required by claim 1. For example, the connection hole (29) does not form part of the guard ring (GR) shown in Figure 3 of *Suwanai et al.* Instead, the connection hole (29) is simply a "hole" that has been "apertured in the silicon oxide film 27 and the BPSG film 17" (col. 8, lines 21-24; emphasis added). The connection hole (29) cannot "cover[] a side face of" either of the films (17, 27), as required by claim 1 (emphasis added), nor is there any teaching or suggestion that the connection hole (29) is "at least near four corners," as required by claim 1 (emphasis added).

Thus, *Suwanai et al.* fails to teach or suggest "a conductor which covers a side face of the first insulating film at least near four corners of the semiconductor substrate ...; and a second insulating film covering [an] outer side face of the conductor," as recited in claim 1.

Wolf et al. and *Kishida et al.* do not make up for this deficiency of *Suwanai et al.*, and the Examiner does not rely on *Wolf et al.* or *Kishida et al.* for any teaching or suggestion of "a conductor which covers a side face of the first insulating film at least near four corners of the semiconductor substrate ...; and a second insulating film covering [an] outer side face of the conductor," as recited in claim 1.

Wolf et al. teaches: "Interconnect delay can be reduced not only by decreasing R of the conductor structures in ICs, but also by decreasing C of the dielectric layers. The value of C, in turn, can be reduced by using dielectric materials with smaller permittivity values (i.e., *low-k dielectric materials*)" (pg. 791, paragraph 1). "[U]ltra-low *k* dielectric materials were ... being investigated for their suitability as IC interconnect layers" (pg. 794, paragraph 6).

Kishida et al. teaches, referring to Figures 7A, 7B, 8A, and 8B, that "a barrier layer composed of a first tantalum nitride film 202 and a first β-tantalum film 203 ... is formed on the bottom and the walls of [an] interconnect groove of [an] insulating film 201. Then, after forming a first copper seed layer 204 on the first β-tantalum film 203, the first copper seed layer 204 is grown through the electroplating, so as to form a first copper plating layer 205." (Col. 8, lines 23-35.)

Moreover, the combination of *Suwanai*, *Wolf*, and *Kishida* does not lead to claim 1. In *Suwanai*, the insulating films 20, 23, 17, and 27 inside the GR (guard ring) and the insulating films 20, 23, 17, and 27 outside the GR are formed at the same time respectively. Thereafter, the GR is formed to be buried into an etched trench in the insulating films 20, 23, 17, and 27. In other wards, *Suwanai* does not disclose nor

suggest that the insulating films 20, 23, 17, and 27 inside the GR and the insulating films 20, 23, 17, and 27 outside the GR be formed individually. Therefore, the combination of *Suwanai* and *Wolf* merely suggests that the insulating films 20, 23, 17, and 27 inside the GR together with the insulating films 20, 23, 17, and 27 outside the GR are insulating films having a relative dielectric constant of 3.8 or less. Accordingly, Claim 1 is not unpatentable over *Suwanai* in view of *Wolf* further in view of *Kishida.*

Moreover, in a case that the insulating films 20, 23, 17, and 27 outside the GR are insulating films having a relative dielectric constant of 3.8 or less, they may be damaged to have cracks or peeling when the semiconductor wafer is diced.

Thus, since *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.* do not teach or suggest, alone or in combination, each and every element of claim 1, claim 1 and claims 2, 7, 9, 11, 13, and 15, which depend therefrom, are allowable over *Suwanai et al.*, *Wolf et al.*, and *Kishida et al.* under § 103(a).

CONCLUSION

In view of the foregoing remarks, Applicants respectfully request reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to Deposit Account No. 06-0916.

Respectfully submitted,

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